Photocouplers Infrared LED & Photo IC

TLP5214A

Isolated IGBT/Power MOSFET gate drive

AC and brushless DC motor drives

Industrial Inverters and Uninterruptible Power Supply (UPS)

Unit**:** mm

The TLP5214A is a highly integrated 4.0 A output current IGBT gate drive photo-coupler housed in a long creepage and clearance SO16L package.

The TLP5214A, a smart gate driver photocoupler, includes functions of IGBT desaturation detection, isolated fault status feedback, soft IGBT turn-off, active Miller cramping and under voltage lockout (UVLO). Moreover, this phorocoupler has features of the desaturation leading edge blanking time, filtering time, and optimisation of the soft-shutdown performance for secure operation of applications. This photocoupler is suitable for driving IGBT and power MOSFET used in inverter applications.

The TLP5214A consists two infrared LEDs and two high-gain and high-speed ICs. They realize high current, high-speed output control

and output fault status feedback.

TOSHIBA   11-10M1

Weight**:** 0.37 g (typ.)

- Peak output current: ±4.0 A (max)
- Guaranteed performance over temperature**:**   -40 to 110 °C
- Supply current: 3.8 mA (max)
- Power supply voltage: 15 V to 30 V
- Threshold input current: 6 mA (max)
- Propagation delay time: 150 ns (max)
- DESAT leading edge blanking time: 1.1 μs (typ.)
- Common-mode transient immunity: ±35 kV/μs (min)
- Isolation voltage: 5000 Vrms (min)
- UL-recognized : UL 1577, File No.E67349
- cUL-recognized :CSA Component Acceptance Service
  No. 5A, File No.E67349
- VDE approved: EN 60747-5-5, EN 62368-1 (Note 1)
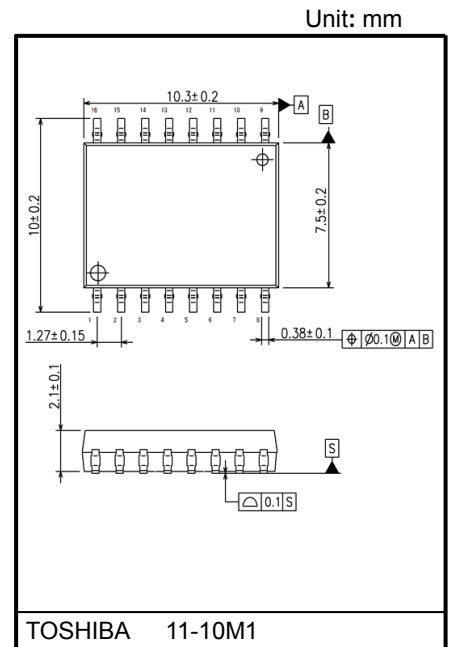
- Construction mechanical rating

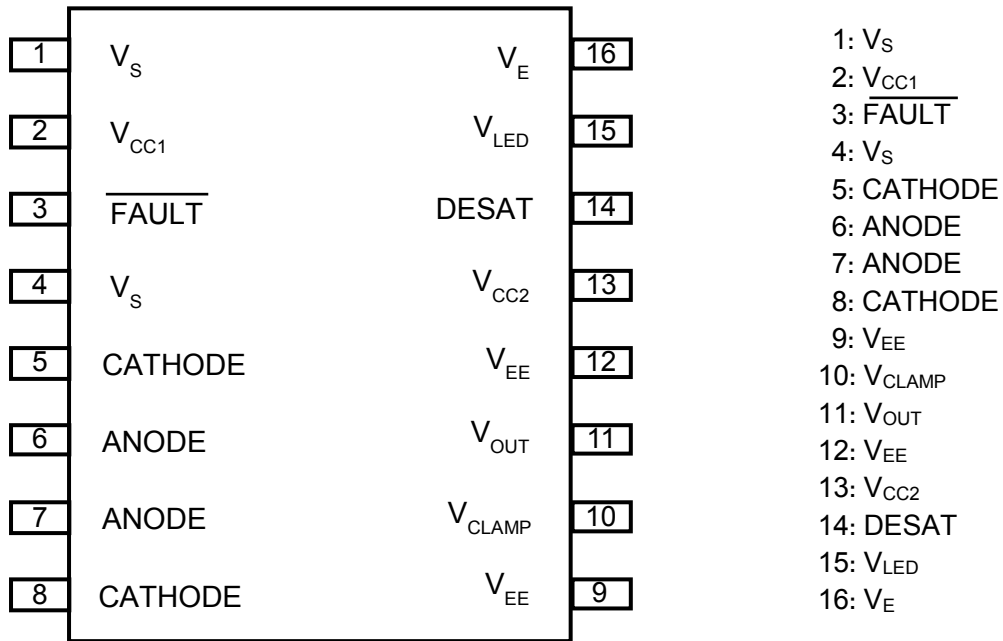|	SO16L
Height	2.3 mm (max)
Creepage Distance	8.0 mm (min)
Clearance	8.0 mm (min)
Insulation Thickness	0.4 mm (min)

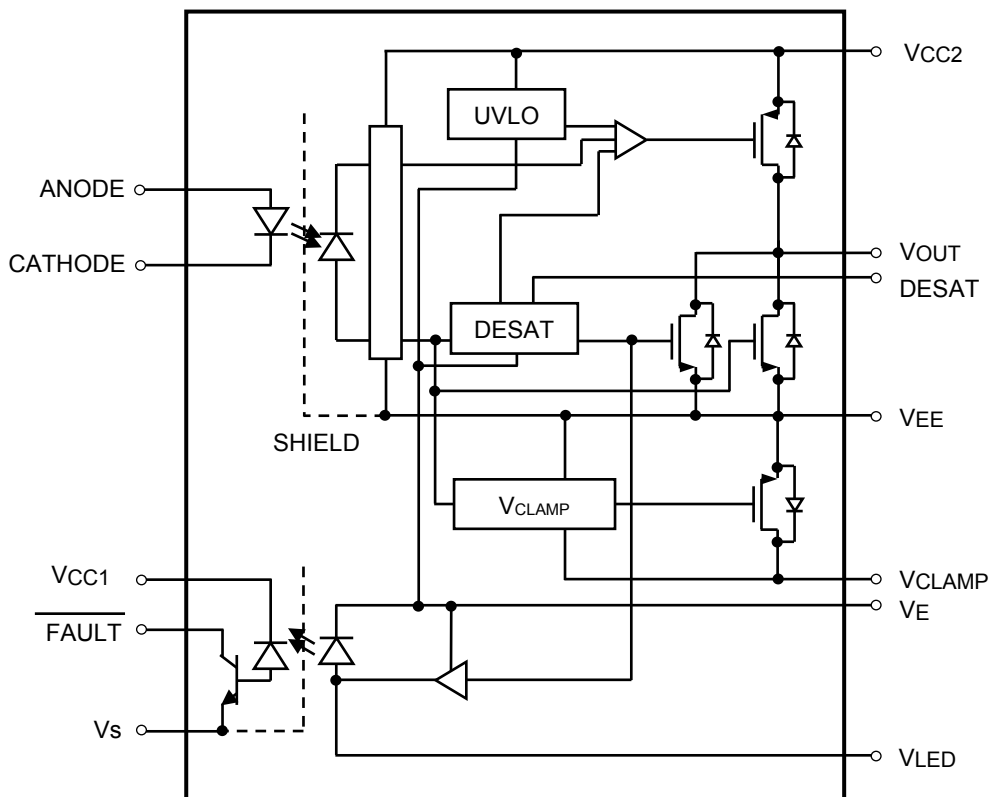Note 1: When a VDE approved type is needed, please designate the **Option(D4).**

Truth Table

I_F	UVLO (V_{CC2}-V_E)	DESAT (14Pin DESAT Terminal Input)	FAULT (3Pin FAULT Terminal Output)	V_O
OFF	Not Active (> V_{UVLO}^+)	Not Active	High	Low
ON	Not Active (> V_{UVLO}^+)	Low (< $V_{DESATth}$)	High	High
ON	Not Active (> V_{UVLO}^+)	High (> $V_{DESATth}$)	Low (FAULT)	Low
ON	Active (< V_{UVLO}^-)	Not Active	High	Low
OFF	Active (< V_{UVLO}^-)	Not Active	High	Low

Start of commercial production
2017-03

Pin Configuration (top view)

Pin	Name
1	V_S
2	V_{CC1}
3	$\overline{FAULT}$
4	V_S
5	CATHODE
6	ANODE
7	ANODE
8	CATHODE
9	V_{EE}
10	V_{CLAMP}
11	V_{OUT}
12	V_{EE}
13	V_{CC2}
14	DESAT
15	V_{LED}
16	V_E

Pins (left side, top to bottom): 1 V_S, 2 V_{CC1}, 3 $\overline{FAULT}$, 4 V_S, 5 CATHODE, 6 ANODE, 7 ANODE, 8 CATHODE

Pins (right side, top to bottom): 16 V_E, 15 V_{LED}, 14 DESAT, 13 V_{CC2}, 12 V_{EE}, 11 V_{OUT}, 10 V_{CLAMP}, 9 V_{EE}

Internal Circuit

Note: A 1-μF bypass capacitor must be connected between pins 9 and 13, pins 13 and 16.

2019-10-30

Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25 °C)

	Characteristics		Symbol	Rating	Unit
LED	Input forward current		I_F	25	mA
	Input forward current derating (Ta ≥ 95°C)		$\Delta I_F/\Delta Ta$	-1	mA/°C
	Peak transient input forward current (Note 1)		I_{FPT}	1	A
	Peak transient input forward current derating (Ta ≥ 95°C)		$\Delta I_{FPT}/\Delta Ta$	-25	mA/°C
	Reverse input voltage		V_R	6	V
	Input power dissipation		P_D	145	mW
	Input power dissipation derating (Ta ≥ 95°C)		$\Delta P_D/\Delta Ta$	-5.0	mW/°C
Detector	Positive input supply voltage		V_{CC1}	-0.5 to 7	V
	"H" peak output current	Ta = -40 to 110 °C	I_{OPH}	-4.0	A
	"L" peak output current	(Note 2)	I_{OPL}	+4.0	A
	$\overline{FAULT}$ output current		$I_{\overline{FAULT}}$	8	mA
	$\overline{FAULT}$ pin voltage		$V_{\overline{FAULT}}$	-0.5 to V_{CC1}	V
	Total output supply voltage		$(V_{CC2}-V_{EE})$	-0.5 to 35	V
	Negative output supply voltage		(V_E-V_{EE})	-0.5 to 15	V
	Positive output supply voltage		$(V_{CC2}-V_E)$	-0.5 to 35 - (V_E-V_{EE})	V
	Output voltage		V_O	-0.5 to V_{CC2}	V
	Peak clamping sinking current		I_{Clamp}	1.7	A
	Miller clamping pin voltage		V_{Clamp}	-0.5 to V_{CC2}	V
	DESAT voltage		V_{DESAT}	V_E to V_E + 10	V
	Output power dissipation		P_O	410	mW
	Output power dissipation derating (Ta ≥ 95°C)		$\Delta P_O/\Delta Ta$	-14.0	mW/°C
Common	Operating temperature range		Topr	-40 to 110	°C
	Storage temperature range		Tstg	-55 to 125	°C
	Lead soldering temperature (10 s) (Note 3)		Tsol	260	°C
	Isolation voltage (AC, 60 s, R.H. ≤ 60%) (Note 4)		BV_S	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note: A ceramic capacitor (1 μF) should be connected between pins 9 and 13, pins 13 and 16 to stabilize the operation of the high gain linear amplifier. Furthermore, in case V_E - V_{EE} > 0 V, a bypass capacitor, which has good high frequency characteristic, a ceramic capacitor (1 μF) should be connected between pins 9 and 16. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: Pulse width P_W ≤ 1 μs, 300 pps

Note 2: Exponential waveform pulse width P_W ≤ 0.2 μs, f ≤ 15 kHz, V_{CC2} = 15 V

Note 3: For the effective lead soldering area.

Note 4: This device considered a two-terminal device: All pins on the LED side are shorted together, and all pin on the photodetector side are shorted together.

Recommended Operating Conditions (Note)

Characteristics	Symbol	Min	Typ.	Max	Unit
Total output supply voltage (Note 1)	$(V_{CC2}-V_{EE})$	15	-	30	V
Negative output supply voltage	(V_E-V_{EE})	0	-	15	V
Positive output supply voltage	$(V_{CC2}-V_E)$	15	-	$30 - (V_E-V_{EE})$	V
Positive input supply voltage	V_{CC1}	3.3	-	5.5	V
Input on-state current (Note 2)	$I_{F(ON)}$	7.5	-	10	mA
Input off-state voltage	$V_{F(OFF)}$	0	-	0.8	V
Operating frequency (Note 3)	f	-	-	50	kHz

Note**:** Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 1: If the V_{CC2} rise slope is sharp, an internal circuit might not operate with stability. Please design the V_{CC2} rise slope under 3.0 V / μs.

Note 2: Input signal rise time (fall time) ≤ 0.5 μs.

Note 3: Exponential waveform. I_{OPH} ≥ -4.0 A (≤ 90 ns), I_{OPL} ≤ 4.0 A (≤ 90 ns), Ta = 110 °C

Electrical Characteristics (Note)

(Unless otherwise specified, Ta = -40 to 110 °C, V_{CC2} - V_{EE} = 15 to 30 V, V_E - V_{EE} = 0 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	V_F	—	I_F = 10 mA, Ta = 25°C	1.4	-	1.7	V
Input reverse current	I_R	—	V_R = 5 V	-	-	10	μA
Input capacitance	C_t	—	V = 0 V, f = 1 MHz, Ta = 25 °C	-	95	-	pF
FAULT low level output voltage	$V_{\overline{FAULT}L}$	—	$I_{\overline{FAULT}}$ = 1.1 mA, V_{CC1} = 5.5 V	-	0.2	0.4	V
			$I_{\overline{FAULT}}$ = 1.1 mA, V_{CC1} = 3.3 V	-	0.2	0.4	
FAULT high level output current	$I_{\overline{FAULT}H}$	—	$V_{\overline{FAULT}}$ = 5.5 V, V_{CC1} = 5.5 V, Ta = 25 °C	-	-	0.5	μA
			$V_{\overline{FAULT}}$ = 5.5 V, V_{CC1} = 3.3 V, Ta = 25 °C	-	-	0.3	
High level output current (Note 1)	I_{OPH}	1	V_O = V_{CC2} - 4 V	-	-4.0	-1.2	A
			V_O = V_{CC2} - 7 V	-	-6.5	-3.0	
Low level output current (Note 1)	I_{OPL}	2	V_O = V_{EE} + 2.5 V	1.2	3.5	-	
			V_O = V_{EE} + 7 V	3	5.5	-	
Low level output current during fault condition	I_{OLF}	—	V_O - V_{EE} = 14 V	90	150	230	mA
High level output voltage	V_{OH}	3	I_O = -100 mA	V_{CC2}-0.3	V_{CC2}-0.1	-	V
Low level output voltage	V_{OL}	4	I_O = 100 mA	-	0.1	0.2	
Clamp pin threshold voltage	V_{tClamp}	—	—	-	2.5	-	
Clamp low level sinking current	I_{CL}	—	V_O = V_{EE} + 2.5 V	0.56	1.8	-	A
High level supply current	I_{CC2H}	5	I_O = 0 mA	-	2.4	3.8	mA
Low level supply current	I_{CC2L}	6	I_O = 0 mA	-	2.3	3.8	
Blanking capacitor charging current	I_{CHG}	7	V_{DESAT} = 2 V	-0.33	-0.24	-0.13	
Blanking capacitor discharge current	I_{DSCHG}	8	V_{DESAT} = 7 V	10	49	-	
DESAT threshold voltage	V_{DESAT}	—	V_{CC2} - V_E > V_{UVLO-}	5.9	6.5	7.5	V
UVLO threshold voltage	V_{UVLO}^+	9	V_O > 5 V	10.5	11.6	13.5	
	V_{UVLO}^-	9	V_O < 5 V	9.2	10.3	11.1	
UVLO hysteresis	$UVLO_{HYS}$	—	—	-	1.3	-	
Threshold input current (L/H)	I_{FLH}	10	V_{CC2} = 30 V, V_O < 5 V	-	2.6	6	mA
Threshold input voltage (H/L)	V_{FHL}	—	V_{CC2} = 30 V, V_O > 5 V	0.8	-	-	V

Note: All typical values are at Ta = 25 °C

Note: This product is more sensitive than conventional products to electrostatic discharge ESD owing to its low power consumption design.

It is therefore all the more necessary to observe general precautions regarding ESD when handling this component.

Note 1: I_O application time ≤ 50 μs, 1 pulse

Isolation Characteristics (Note) (Ta = 25 °C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Capacitance input to output	C_S	Vs = 0 V, f = 1 MHz	-	1.0	-	pF
Isolation resistance	R_S	R.H. ≤ 60 %, V_S = 500 V	10^{12}	10^{14}	-	Ω
Isolation voltage	BV_S	AC, 60 s	5000	-		Vrms

Note: This device considered a two-terminal device: All pins on the LED side are shorted together, and all pin on the photodetector side are shorted together.

Switching Characteristics (Note)
(Unless otherwise specified, Ta = -40 to 110 °C, V_{CC2} - V_{EE} = 15 to 30 V, V_E - V_{EE} = 0 V)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Propagation delay time (Note 1)	L → H	t_{pLH}	11	R_g = 10 Ω, C_g = 25 nF, V_{CC2} = 30 V	I_F = 0 → 10 mA	50	85	150	ns
	H → L	t_{pHL}			I_F = 10 → 0 mA	50	90	150	
Output rise time (10-90 %) (Note 1)		tr			I_F = 0 → 10 mA	-	32	-	
Output fall time (90-10 %) (Note 1)		tf			I_F = 10 → 0 mA	-	18	-	
Pulse with distortion (Note 1)		| t_{pHL}-t_{pLH} |			I_F = 0 ↔ 10 mA	-	-	50	
Propagation delay skew (device to device) (Note 1) (Note 2)		t_{psk}			I_F = 0 ↔ 10 mA	-80	-	80	
DESAT sense to 90% delay		$t_{DESAT(90\%)}$	12	C_{DESAT} = 100 pF, R_g = 10 Ω, V_{CC2} = 30 V, R_F = 2.1 kΩ, V_{CC1} = 5 V	Cg = 25 nF	-	230	500	μs
DESAT sense to 10% delay		$t_{DESAT(10\%)}$			Cg = 25 nF	-	7.0	8.5	
					Cg = 10 nF	-	2.5	3.5	
DESAT leading edge blanking time		$t_{DESAT(LEB)}$				-	1.1	-	ns
DESAT filter time		$t_{DESAT(FILTER)}$				-	90	-	
DESAT sense to low level FAULT signal delay		$t_{DESAT(FAULT)}$		-		-	350	550	ns
DESAT sense to low propagation delay		$t_{DESAT(LOW)}$				-	200	-	
DESAT input mute		$t_{DESAT(MUTE)}$				7	20	-	
RESET to high level FAULT signal delay		$t_{RESET(FAULT)}$		C_{DESAT} = 100 pF, R_g = 10 Ω, V_{CC2} = 30 V, R_F = 2.1 kΩ, V_{CC1} = 5.5 V		0.2	0.6	2	μs
High-level Common-mode transient immunity (Note 3)		CM_H	13 to 16	T_a = 25 °C, R_g = 10 Ω, Cg = 25 nF, V_{CC2} = 30 V, R_F = 2.1 kΩ, C_F = 15 pF, V_{CM} = 1500 V_{p-p}	$V_{O (min)}$ = 26 V, $V_{FAULT(min)}$ = 2 V	±35	-	-	kV/μs
Low-level Common-mode transient immunity (Note 4)		CM_L			$V_{O (max)}$ = 1 V, $V_{FAULT(max)}$ = 0.8 V	±35	-	-	

Note: All typical values are at T_a = 25 °C.

Note 1: Input signal (f = 10 kHz, duty = 50%, tr = tf = 5 ns or less)
C_L is approximately 15 pF which includes probe and stray wiring capacitance.

Note 2: The propagation delay skew, t_{psk}, is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

Note 3: CM_H is the maximum rate of fall of the common mode voltage that can sustained with the output voltage in the logic high state (V_O > 26 V or V_{FAULT} > 2 V).

Note 4: CM_L is the maximum rate of rise of the common mode voltage that can sustained with the output voltage in the logic low state (V_O < 1 V or V_{FAULT} < 0.8 V).

Test Circuit

Test Circuit 1: I$_{OPH}$
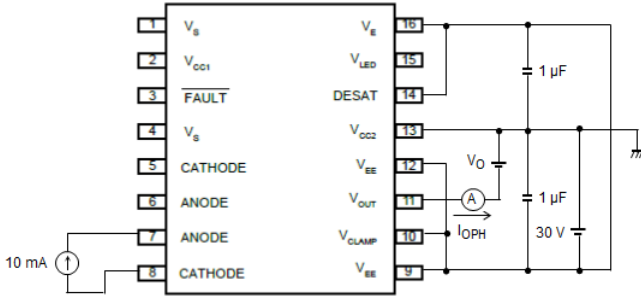
Test Circuit 2: I$_{OPL}$

Test Circuit 3: V$_{OH}$

$$V_{OH} = V_{CC2} - V_O$$
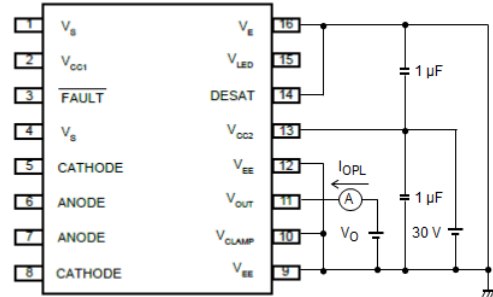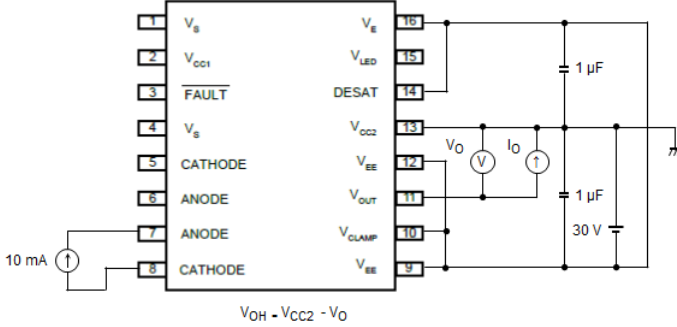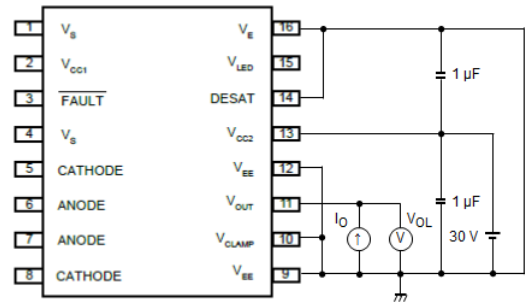
Test Circuit 4: V$_{OL}$

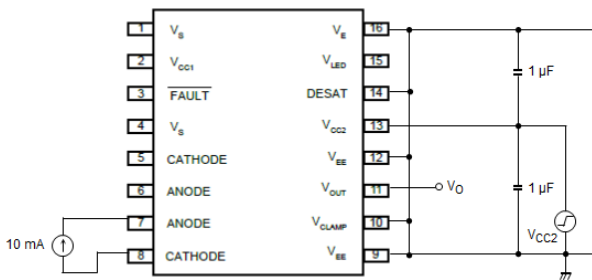### Test Circuit 5: I$_{CC2H}$
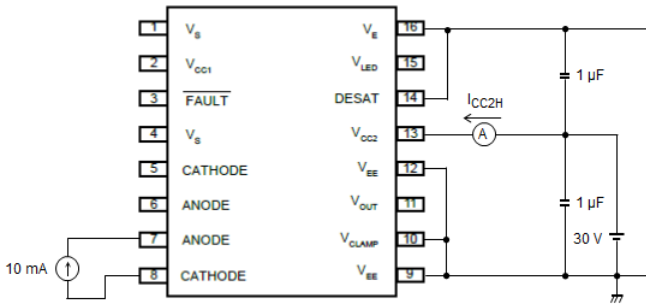
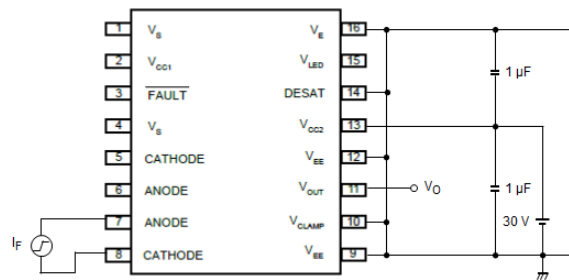### Test Circuit 6: I$_{CC2L}$
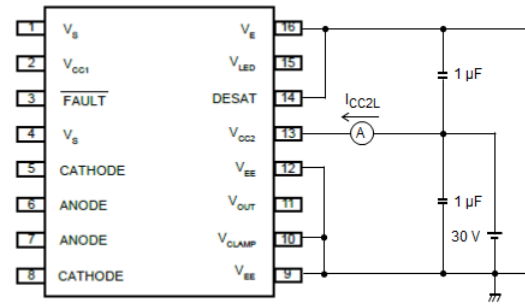
Test Circuit 7: ICHG
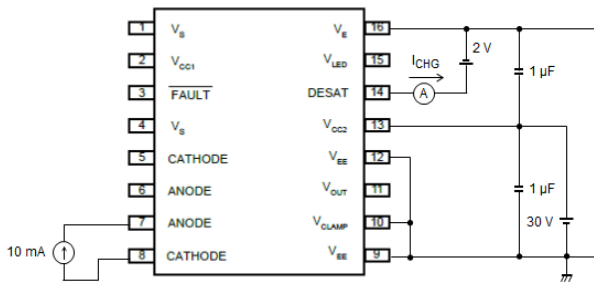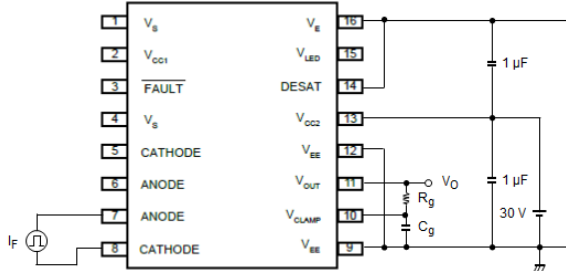

Test Circuit 8: IDSCHG
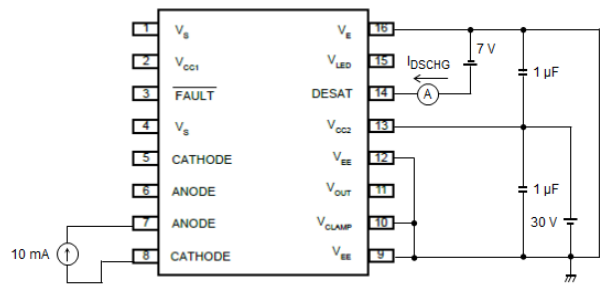
Test Circuit 9: VUVLO

Test Circuit 10: IFLH

Test Circuit 11: tpLH, tpHL, tr, tf, | tpHL-tpLH |

I_F = 10 mA (P.G.)
(f =10 kHz, duty = 50%, rise / fall time 5 ns or less)
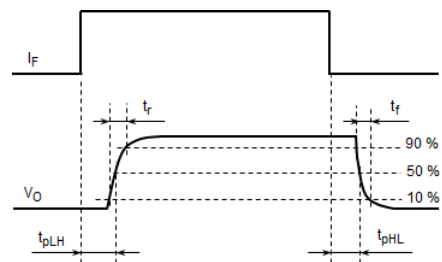
P.G.: Pulse generator

Test Circuit 12: tDESAT(90%), **t**DESAT(10%), **t**DESAT(LEB), **t**DESAT(FILTER), **t**DESAT(FAULT), **t**DESAT(Low), **t**DESAT(MUTE),
tRESET(FAULT)

I_F = 10 mA (P.G.)
(f =10 kHz, duty = 50%, rise / fall time 5 ns or less)

P.G.: Pulse generator

2019-10-30
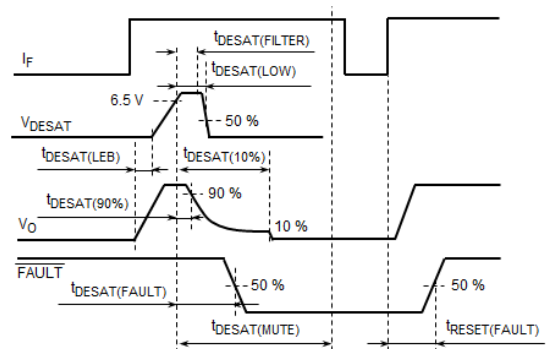
Test Circuit 13: CMR_LED1   ON
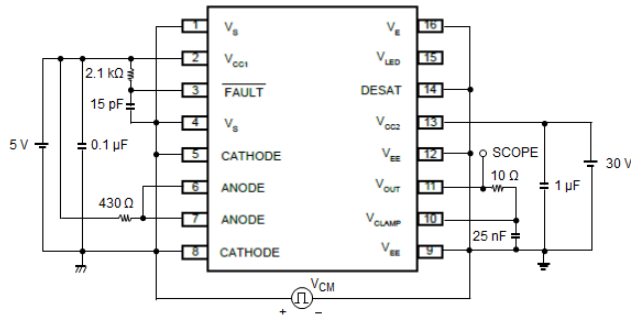
Test Circuit 14: CMR_LED1   OFF
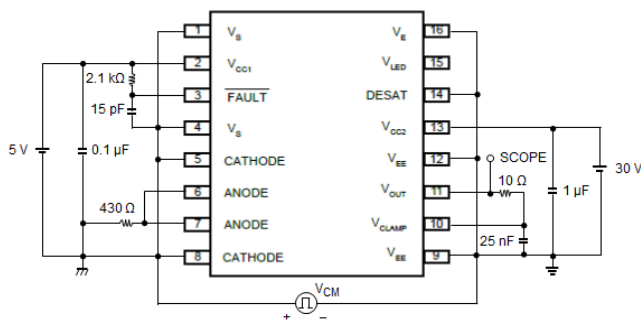
Test Circuit 15: CMR_LED2   ON
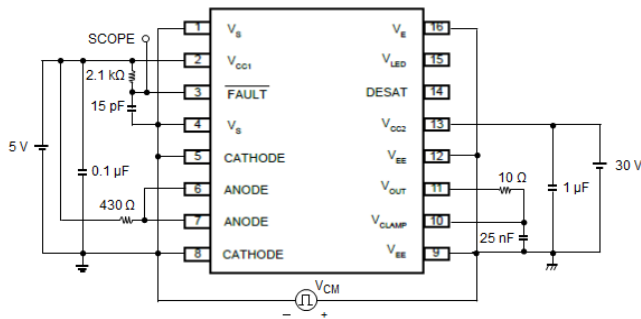
Test Circuit 16: CMR_LED2   OFF
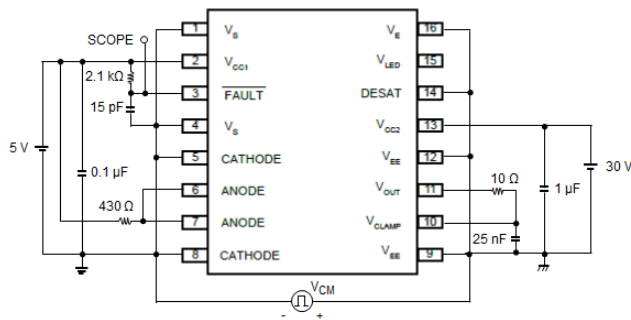
Characteristics Curves (Note)
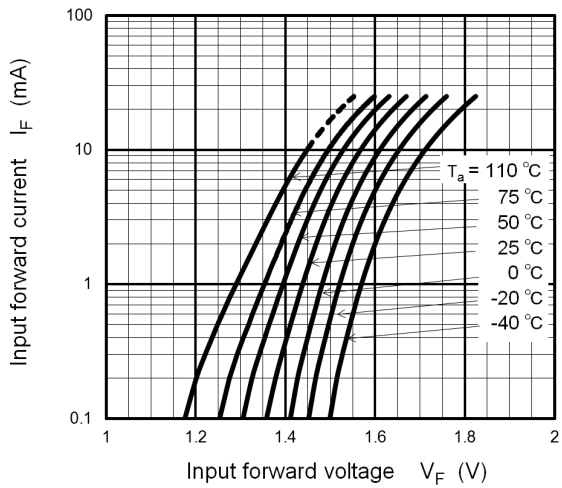
I_F - V_F
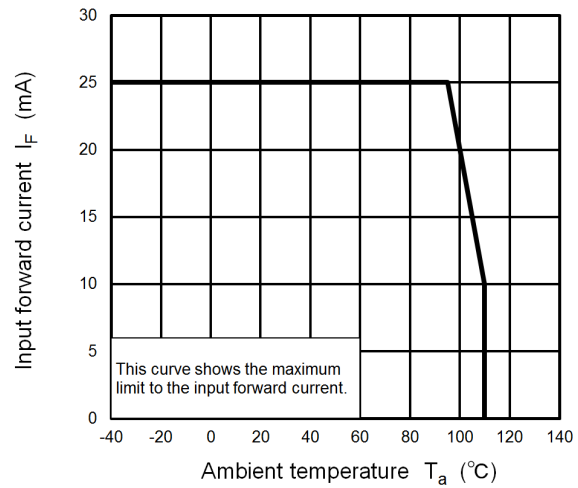
I_F - T_a
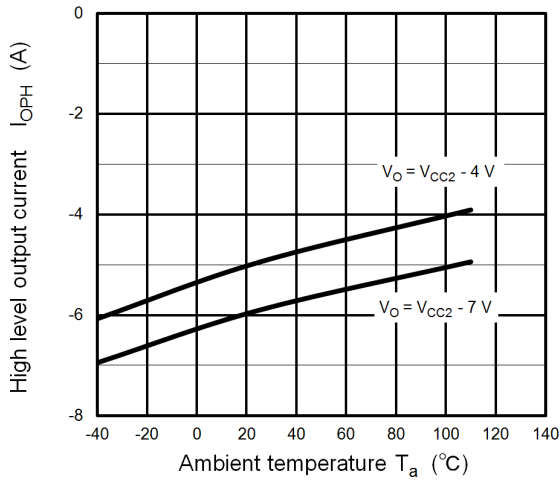
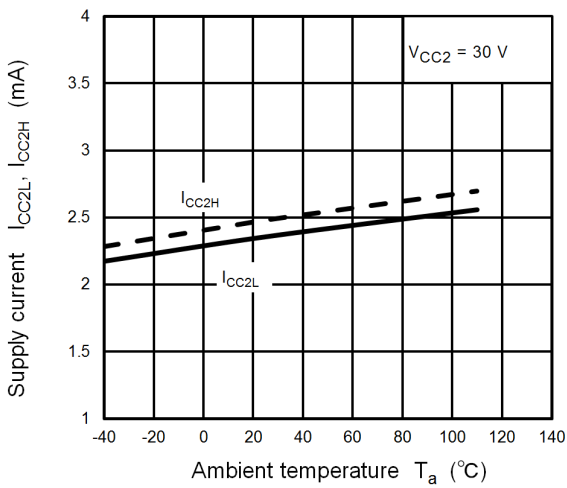

I_{OPH} - T_a
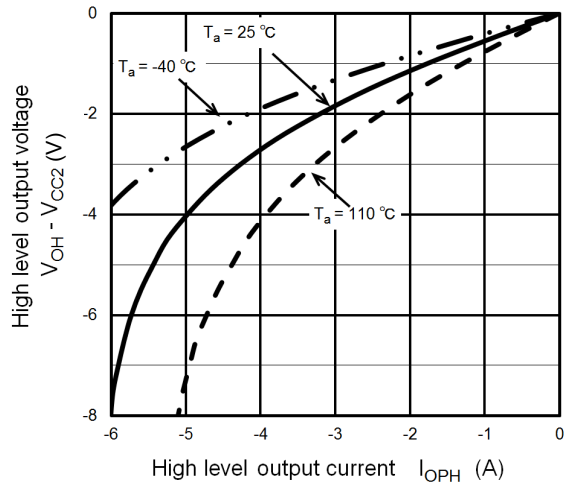
$(V_{OH} - V_{CC2})$ - I_{OPH}
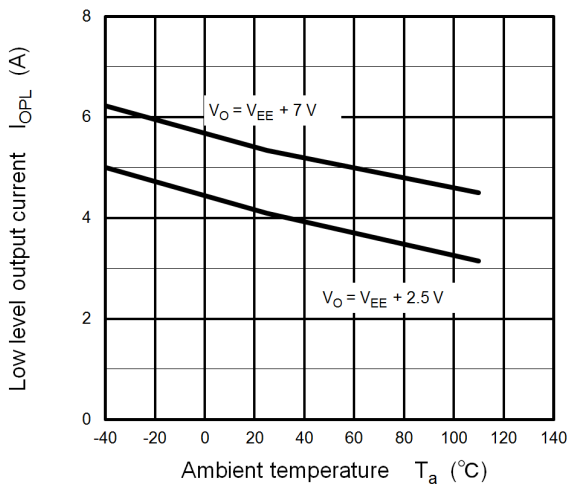
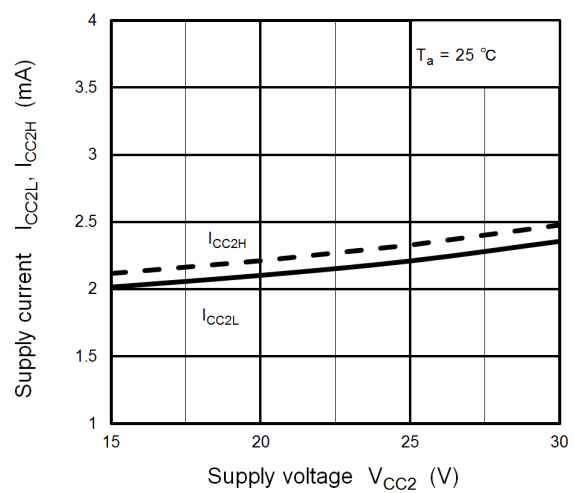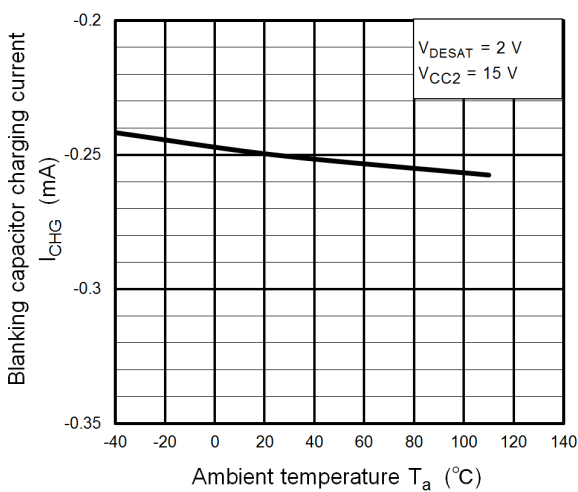
I_{OPL} - T_a
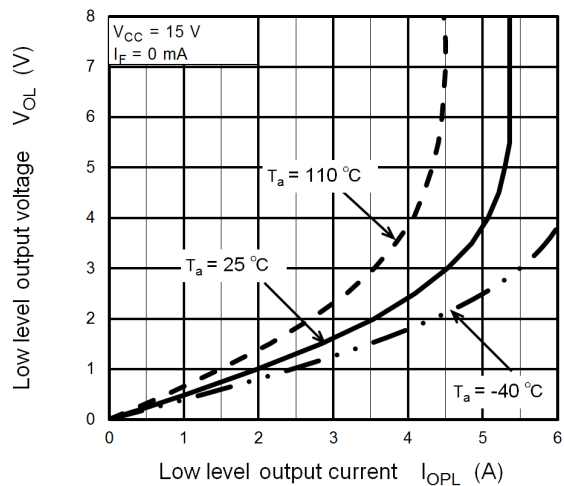
V_{OL} - I_{OPL}
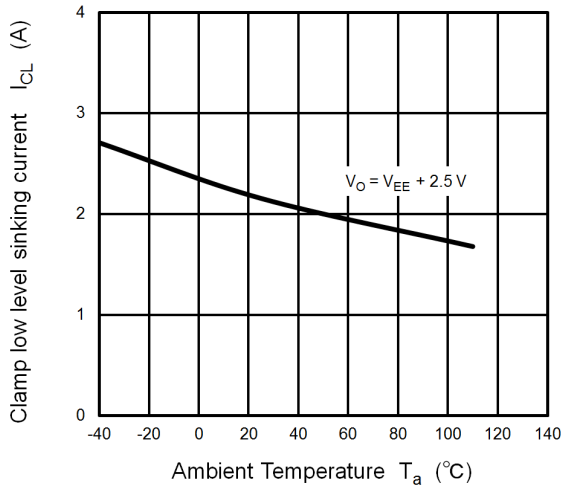
I_{CL} - T_a
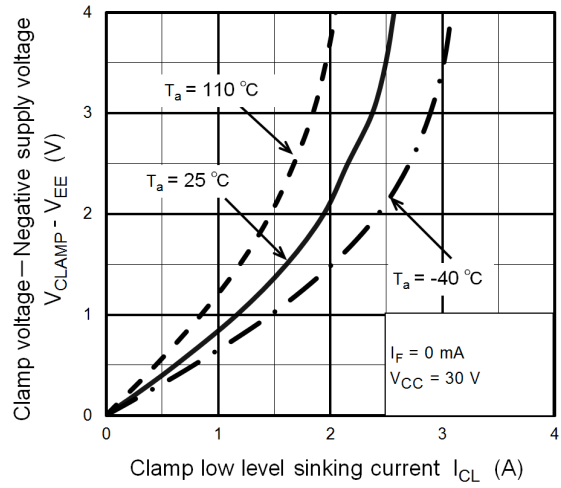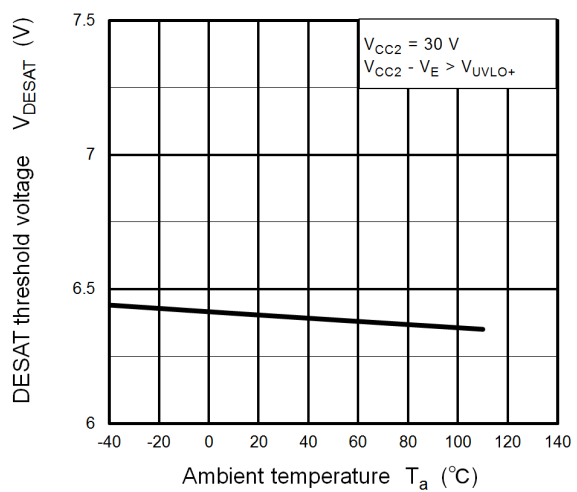

$(V_{CLAMP} - V_{EE})$ - I_{CL}
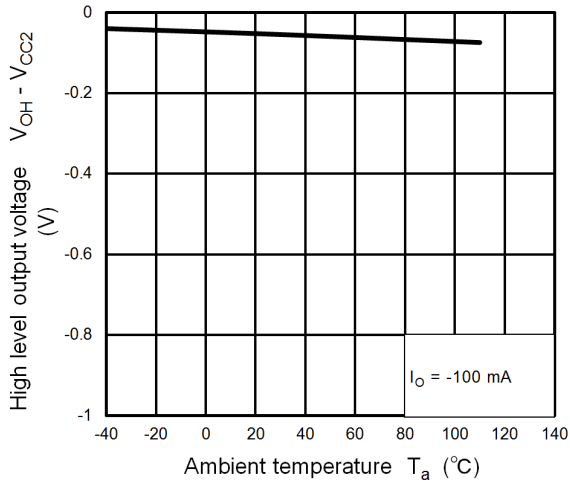

I_{CC2L}, I_{CC2H} - T_a
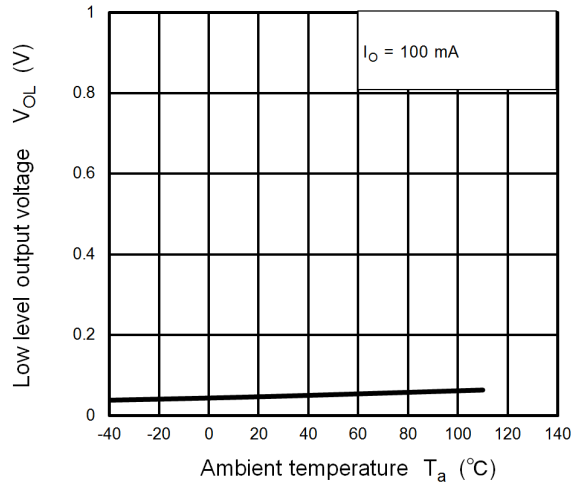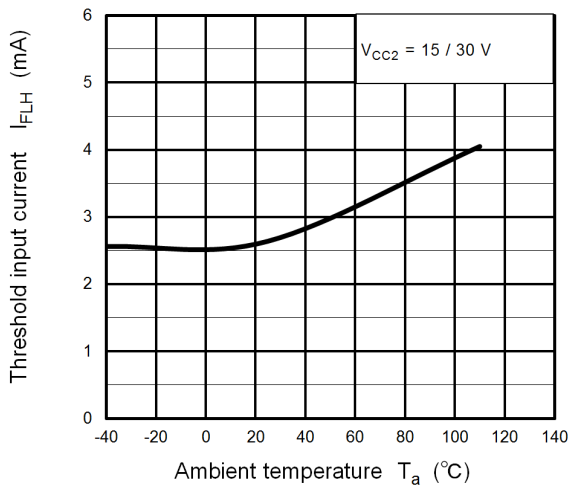

I_{CC2L}, I_{CC2H} - V_{CC2}
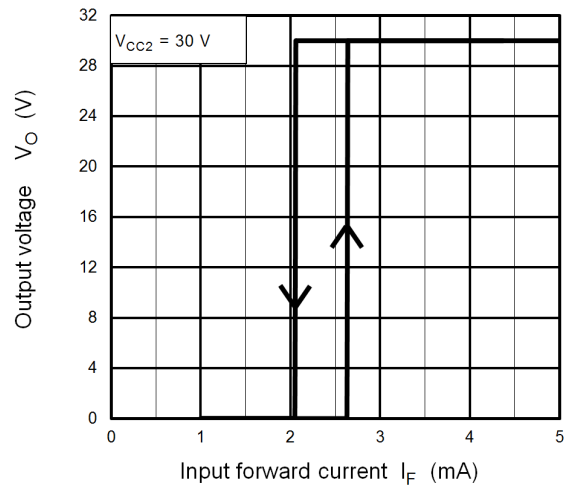

I_{CHG} - T_a

V_{DESAT} - T_a
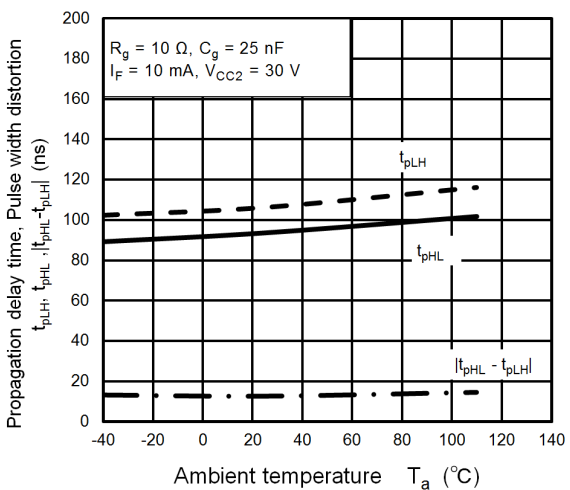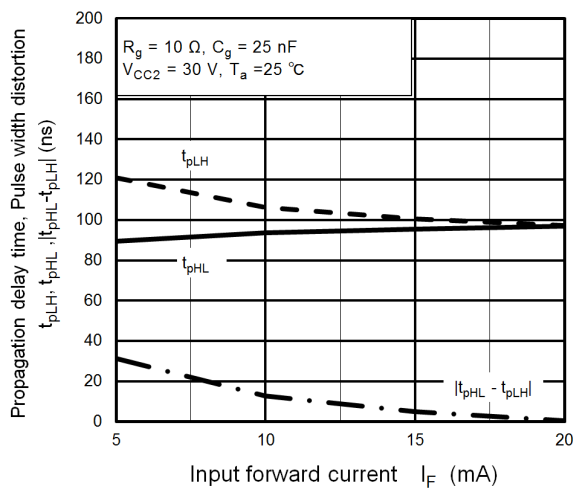
$(V_{OH} - V_{CC2})$ - T_a

V_{OL} - T_a

I_{FLH} - T_a

V_O - I_F

t_{pHL}, t_{pLH}, $|t_{pHL} - t_{pLH}|$ - T_a

t_{pHL}, t_{pLH}, $|t_{pHL} - t_{pLH}|$ - I_F
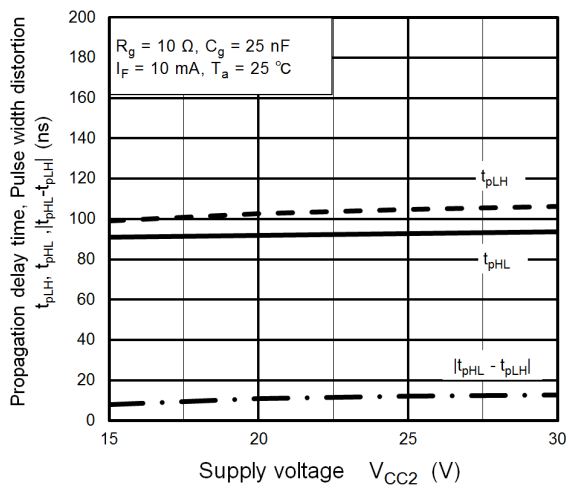
t_{pHL}, t_{pLH}, $|t_{pHL} - t_{pLH}|$ - V_{CC2}
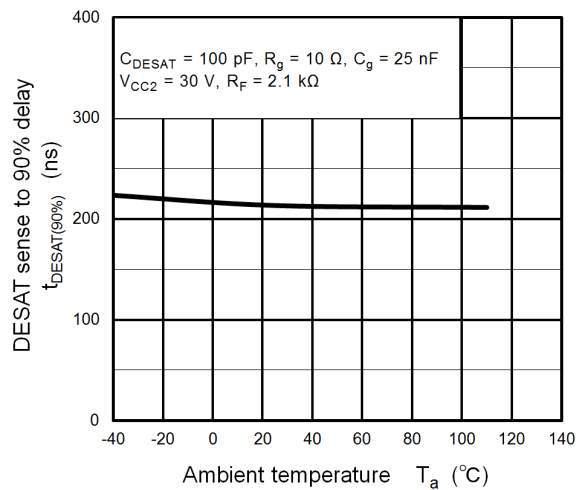
$t_{DESAT(90\%)}$ - T_a
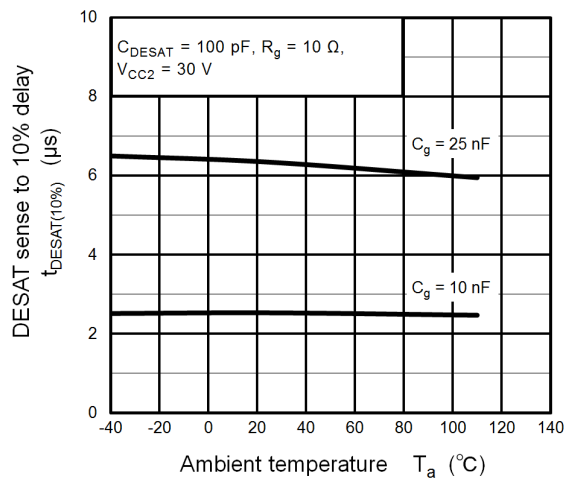
$t_{DESAT(10\%)}$ - T_a

$t_{DESAT(LEB)}$ - T_a

$t_{DESAT(FILTER)}$ - T_a

$t_{DESAT(FAULT)}$ - T_a

$t_{DESAT(LOW)}$ - T_a

$t_{RESET(FAULT)}$ - T_a

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Soldering and Storage

(1) Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

・When using soldering reflow
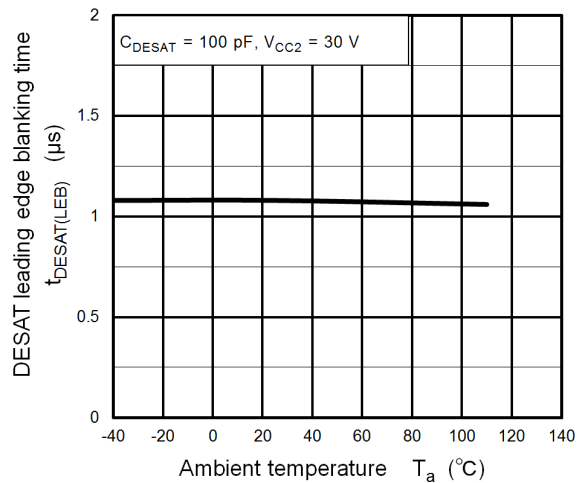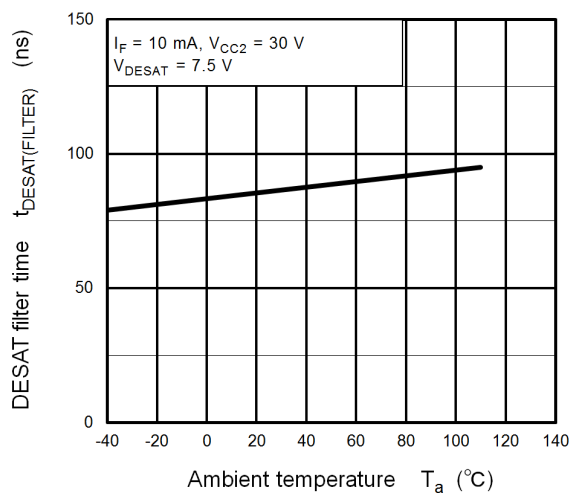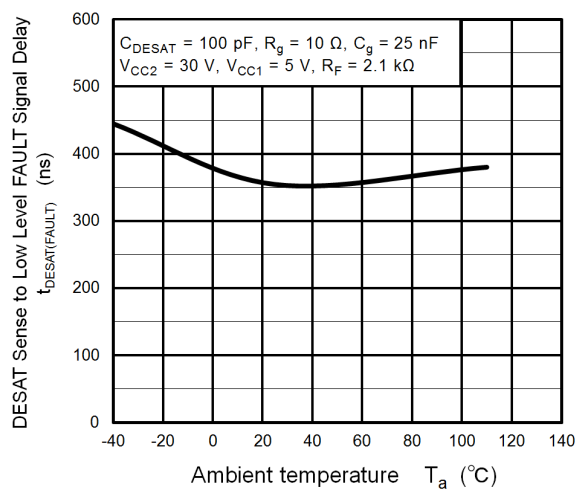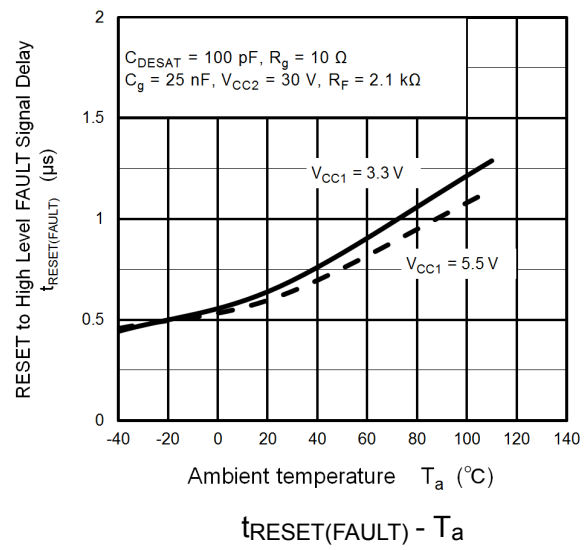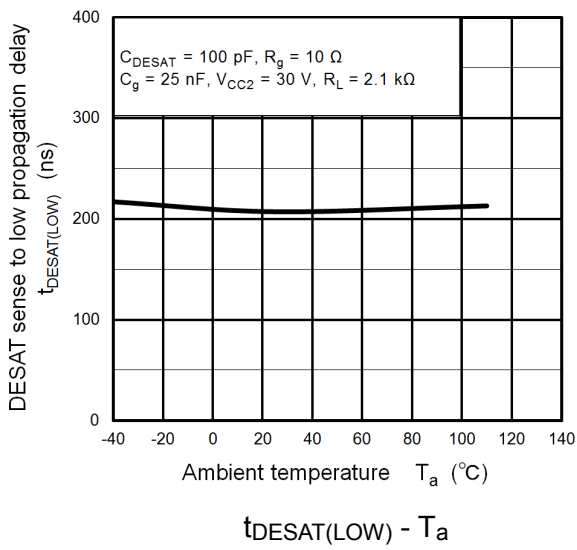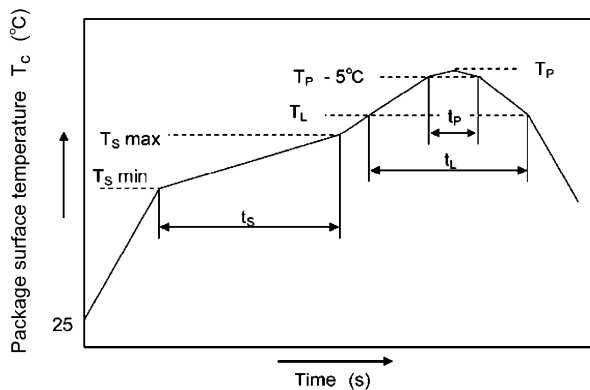 The soldering temperature profile is based on the package surface temperature.
  (See the figure shown below, which is based on the package surface temperature.)
  Reflow soldering must be performed once or twice.
  The mounting should be complicated with the interval from the first to the last mountings being 2 weeks.

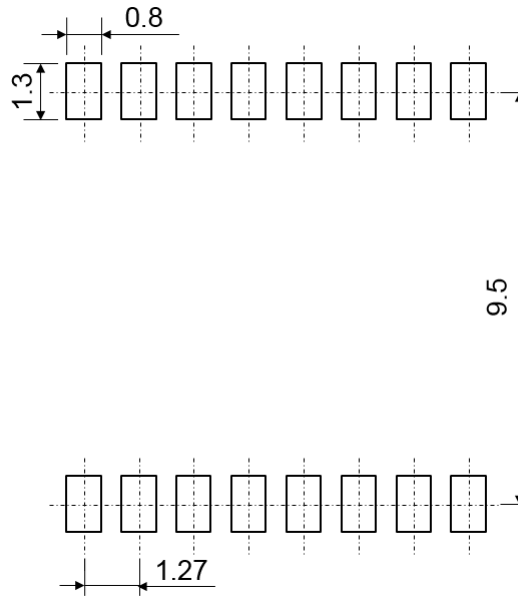|	Symbol	Min	Max	Unit
Preheat temperature	T_S	150	200	°C
Preheat time	t_S	60	120	s
Ramp-up rate (T_L to T_P)			3	°C/s
Liquidus temperature	T_L	217		°C
Time above T_L	t_L	60	150	s
Peak temperature	T_P		260	°C
Time during which T_c is between ($T_P - 5$) and T_P	t_P		30	s
Ramp-down rate (T_P to T_L)			6	°C/s

An example of a temperature profile when lead(Pb)-free solder is used

・When using soldering flow
  Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 150 seconds.
  Mounting condition of 260 °C within 10 seconds is recommended.
  Flow soldering must be performed once.
・When using soldering iron
  Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C.
  Heating by soldering iron must be done only once per lead.

(2) Precautions for General Storage

・Avoid storage locations where devices may be exposed to moisture or direct sunlight.
・Follow the precautions printed on the packing label of the device for transportation and storage.
・Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %.
・Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
・Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation of corrosion, which will deteriorate the solderability of the leads.
・When restoring devices after removal from their packing, use anti-static containers.
・Do not allow loads to be applied directly to devices while they are in storage.
・If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

Land Pattern Dimensions for Reference Only

0.8

1.3

9.5

1.27

Unit: mm

Marking

TLP5214A

J

Lot No.

Part No. (or abbreviation code)

Process lot No.

Country of origin
J; Japan

Pin No. 1
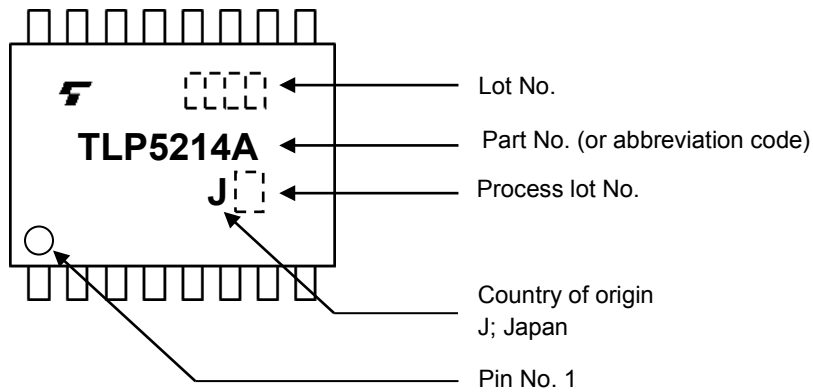
1. Ordering Method

When placing an order, please specify the part number, the tape and the quantity (Multiples of 1500) as shown in the following example.

Example) TLP5214A(TP,E   1500 pcs

    Part number: TLP5214A
    Tape type: TP (12-mm pitch)
    [[G]]/RoHS COMPATIBLE: E (Note 1)
    Quantity (must be a multiple of 1500): 1500 pcs

Note 1：Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.
RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

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